AMENDMENT TO CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1.   (Original) A hierarchical test control network for an integrated circuit, comprising:

a top-level test control circuit block, said top-level test control circuit block comprising a chip access port (CAP) controller; and

a plurality of lower-level test control circuit blocks connected to said top-level test control circuit block in a hierarchical structure, each of said lower-level test control circuit blocks comprising a socket access port (SAP) controller;

wherein test operation is transferred downward and upwards within said hierarchical structure.

Claims 2-14 (Previously cancelled).

15.   (Previously presented) The hierarchical test control network of claim 1, wherein the lower-level test control circuit blocks are connected in a serial chain.

16.   (Previously presented) The hierarchical test control network of claim 1, wherein each of said lower-level test control circuit blocks is connected to a different virtual circuit block for controlling testing thereof.

17.   (Previously presented) The hierarchical test control network of claim 1, wherein each of said lower-level test control circuit blocks comprises a test mode select input port, a test data input port, and a test data output port.

18.   (Previously presented) The hierarchical test control network of claim 1, wherein said top-level test control circuit block and said plurality of lower-level test control circuit blocks are organized in a plurality of tiers.

19.   (Previously presented) The hierarchical test control network of claim 18, wherein all of the lower-level test control circuit blocks connected at a same tier collectively output a common test mode data output signal comprising a logical OR of individual test mode data output signals output from each of the lower-level test control circuit blocks connected at the same tier.

20.   (Previously presented) A hierarchical test control network for an integrated circuit, comprising:

     means for controlling a chip access port (CAP) of a top-level test control circuit block;

     means for controlling a plurality of socket access ports (SAPs) for a plurality of lower-level test control circuit blocks, each lower-level test control circuit block connected to said top-level test control circuit block in a hierarchical structure; and

     means for transferring test operation downward and upwards within said hierarchical structure.

21.   (Previously presented) The hierarchical test control network of claim 20, wherein the lower-level test control circuit blocks are connected in a serial chain.

22.   (Previously presented) The hierarchical test control network of claim 20, wherein each of said lower-level test control circuit blocks is connected to a different virtual circuit block for controlling testing thereof.

23.   (Previously presented) The hierarchical test control network of claim 20, wherein each of said lower-level test control circuit blocks comprises a test mode select input port, a test data input port, and a test data output port.

Claims 24-30 (Cancelled).

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